

High-speed USB2.0 design guideline

Introduction

The purpose of this document is to help designers with a design guideline on the high-speed USB2.0 PCB layout with AT32 MCU.

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1 Overview

High-speed USB2.0 D+/D- differential signals operate at 480 Mbps, equivalent to operating at a fundamental frequency of 240 MHz. At high speed, the amplitude for D+/D- signals are relatively low at 400 mV level. Thus caution must be taken when it comes to the design of high-speed USB2.0 PCB layout.

2 USB2.0 PCB design tips

For the design of PCB layout of high-speed USB2.0, the following rules should be recommended in order to minimize the occurrence of failures as a result of poor signal quality.

2.1 General considerations

- The routing of high-speed USB and relevant components takes priority over others, and should be designed and arranged before any other.
- D+/D- differential paths must be of the same length and placed in parallel, with identical distance apart. In principle, they should be at the same layer to avoid impedance mismatch issue.
- An impedance calculator needs to be used to calculate all PCB parameters to ensure that they meet a 90 Ω requirement of D+/D- paths. It is recommended that the differential signals of high-speed USB are routed at the top or bottom of the PCB, and the ground copper plane is poured on both sides of their copper tracks.

Figure 1 takes an impedance calculator from “JLCPCB” as an example to calculate a two-layer PCB that is 1.6 mm in board thickness and 1 oz in copper weight. If the distance between the both edges of the D+/D- lines is 6 mil, and the either edge of D+/D- line is 6 mil from the edge of copper pouring, the D+/D- line width should be 11.16 mil. PCB parameters and specifications vary from supplier to supplier. Most of PCB manufacturers can offer necessary information for users' reference.

Figure 1. Example of an impedance calculator

嘉立创阻抗计算器(新)

嘉立创层压结构 使用说明

板子层数: 2 成品厚度: 1.6 外层铜厚: 1oz(常用) 计算单位: mil

阻抗表: +添加阻抗 +复制阻抗 删除 计算

需求阻抗 (ohm)	阻抗模式	阻抗层	上参考层	下参考层	线距 (mil)	阻抗线到铜距离 (mil)
90	共面差分阻抗 (外层)	L1	/	L2	6	6

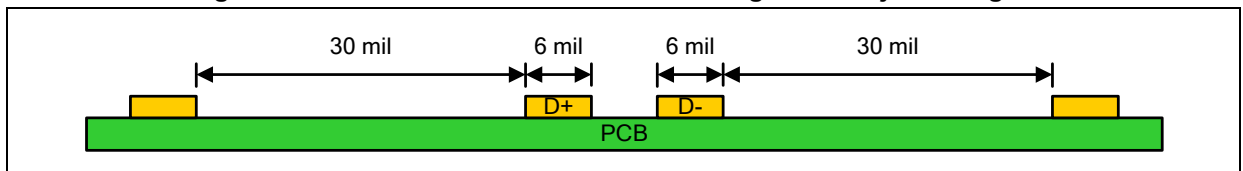
方案一: JLC0216

需求阻抗 (ohm)	阻抗模式	阻抗层	上参考层	下参考层	线宽	线距	阻抗线到铜距离
90	共面差分阻抗 (外层)	L1	/	L2	11.1600	6.0000	6.0000

层名	材料	厚度 (mil)	厚度 (mm)
L1	外层铜厚	1.38	0.0350
芯板	1.5mm 1/10Z含铜 (双面板)	57.68	1.4650
L2	外层铜厚	1.38	0.0350

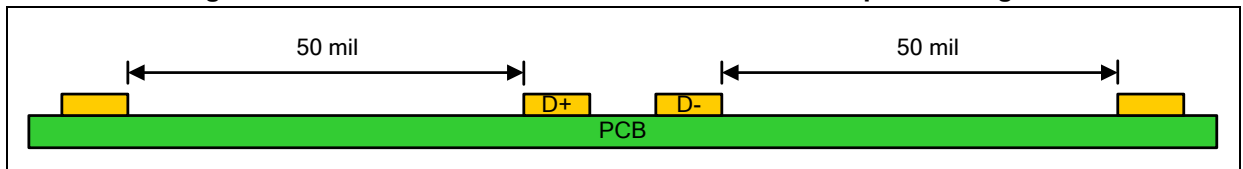
- Minimize the use of vias that are likely to cause impedance change and signal reflection issue as well as interferences from other layers. If vias must be used, it is recommended to reduce the resulting parasitic capacitance by expanding surrounding clear spaces while at the same time ensuring a smooth or unobstructed signal return path. For more, please see section 2.2.
- Keep D+/D- routing away from board edge or ground edge, at least 90 mil apart.
- When there is somewhere D+/D- lines require a rotation of 90 degree, it is recommended to utilize two 45-degree rotation angles or arc routing in order to minimize signal reflection and impedance interruption issue.
- Follow the “5W rule” to design D+/D- tracks and other general adjacent PCB signals. In other words, a distance present between D+/D- tracks and other PCB signals must be at least five times the D+/D- line width, so as to reduce interferences to D+/D- differential signals. For example, if the D+/D- line width is 6 mil, then a minimum of 30 mil must remain between D+/D- tracks and other PCB signals nearby.

Figure 2. Track distance between D+/D- and general adjacent signals



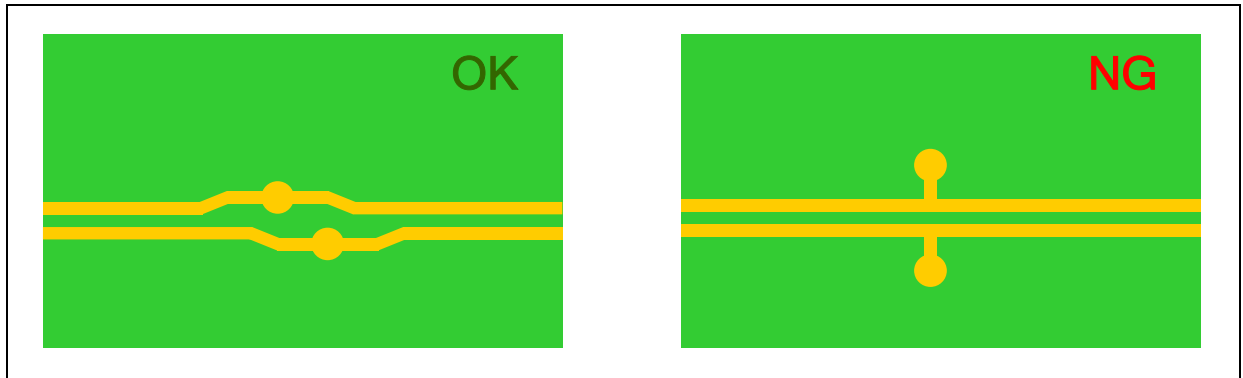
- Keep at least 50 mil between D+/D- tracks and adjacent clocks or periodic signals on the PCB. Keep D+/D- tracks away from other connectors, such as I/Os, control signal, or power connectors.

Figure 3. Track distance between D+/D- and clocks or periodic signals



- Minimize the D+/D- track length if conditions permit. This is particularly important when they are placed in parallel with clocks or periodic signals. USB connectors should be placed as close to chip as possible.
- Keep D+/D- line away from noise sources such as crystals, oscillators, pulse generators, switching powers, or magnetic components.
- Branching on D+/D- tracks should be avoided for this is likely to cause signal reflection issue. Besides, no test points should be placed on D+/D- tracks. If this is unavoidable, signal tracks must directly go through test points, rather than pulling a sub-branch line from D+/D- to place test points. Also the test points should not be formed with vias. If there is a need to put other components such as ESD or overvoltage protection components on D+/D-, the branched D+/D- tracks are prohibited as well.

Figure 4. Example of test point placement



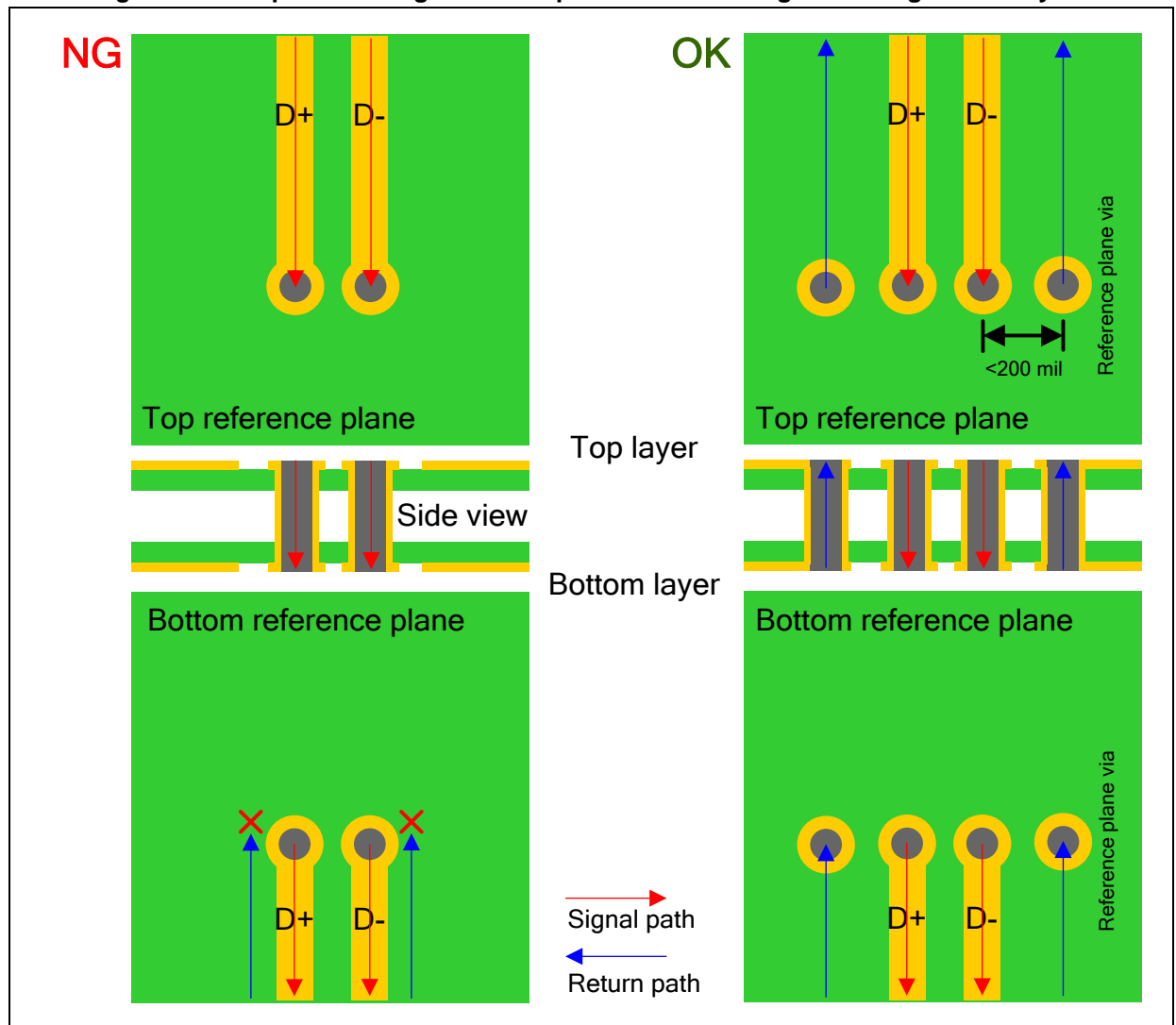
- D+/D- tracks should be routed on the intact copper plane of power or ground. If D+/D- tracks cannot avoid routing through an interrupted copper plane, it is necessary to provide a smooth signal return path, which would otherwise increase noise induction and radiation because of the length disparity between a signal and its return path or interruption of the return path. For more information, see section [2.3](#).
- Place the decoupling capacitors of V_{DD} or V_{BUS} as close to chip's pins as possible. The wider the tracks for V_{DD} or V_{BUS} , the better the result, at least no less than 40 mil. It is also possible to reduce power noise by adding components such as magnetic beads.
- For high-speed USB PHY, an external resistor (error of $\pm 1\%$) is usually required to serve the internal reference current source. Taking AT32F405 series as an example, such resistance is 12 k Ω . The resistor should be placed as close to a chip as possible, with one end of it tied to OTGHS_R and the other to a digital ground plane.
- For additional ESD protection information on USB interface, please refer to AN0034.

2.2 Signal routing across layers of PCB

It is important to ensure that signal return path is intact and complete when high-speed USB signal tracks go through from one layer to the other of PCB. Such consideration should be given even when differential signals use the same layer's copper pouring as a return path.

The entire high-speed USB track from start to end should be routed on the same reference plane. If this is made impossible because signal tracks need to go through different PCB layers, it is necessary to add vias to connect two reference planes so as to make sure the intactness of signal paths. One of the methods is to punch an additional reference plane via, which locates within 200 mil of signal via.

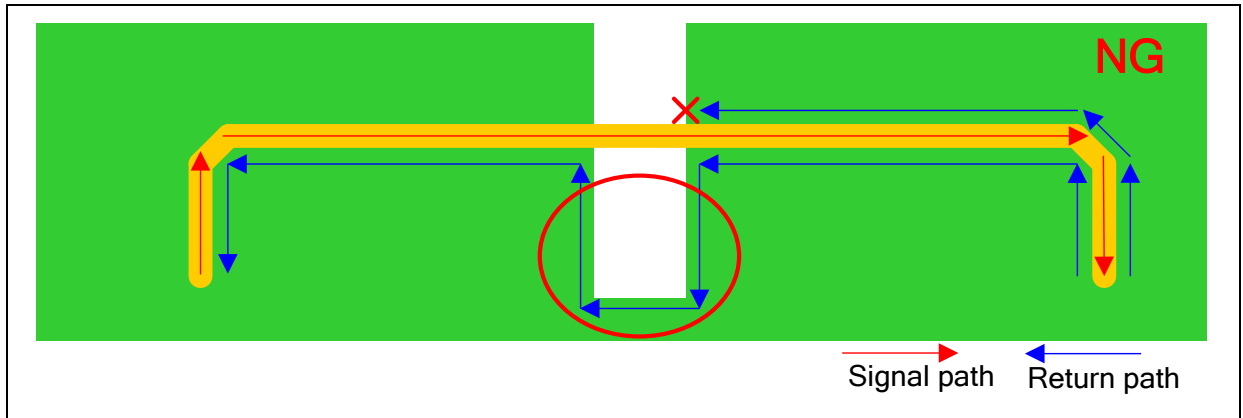
Figure 5. Example of adding reference plane vias when signal routing across layers



2.3 Signal routing over interrupted reference plane

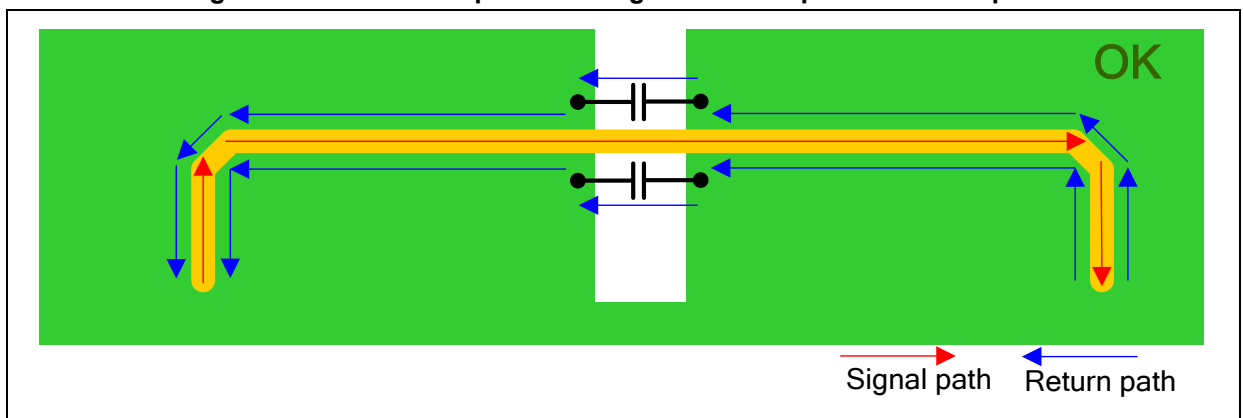
It is important to prevent high-speed USB signal lines from passing through an interrupted reference plane. Thus an intact or unhindered signal loop path must be guaranteed, for not only signal going-out path but also for signal return path, including the commonly used return path – the copper pouring of reference ground or others. [Figure 6](#) shows an example of a high-speed signal track going directly through an interrupted reference plane. In this scenario, on one hand, the return path at the bottom makes a detour, taking a longer route than the signal path. On the other hand, the return path at the top is being interrupted due to discontinuous copper plane.

Figure 6. Incorrect example of routing over interrupted reference plane



If routing an interrupted reference plane cannot be avoided, the signal path must be perpendicular (90 degree) to the plane edge. At the same time, a good return path must be considered. For this, the most common solution is to add a capacitor of 100 nF ~ 1 μ F to either side of the reference plane that are close to signal tracks, with the aim of connecting interrupted reference plane.

Figure 7. Correct example of routing over interrupted reference plane



3 Revision history

Table 1. Document revision history

Date	Revision	Changes
2023.12.20	2.0.0	Initial release

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